DIGITAL LOGIC DESIGN

II B. TECH- II SEMESTER

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	**T**	**P**	**C**	**CIE**	**SEE**	**Total**
A4EC02	**ESC**	3	-	-	3	30	70	100

COURSE OBJECTIVES:

The course should enable the students to:

1. Understand numerical and character representations in digital logic including ASCII and error detecting and correcting codes.
2. Design combinational and sequential logic circuits
3. Optimize combinational and sequential logic circuits.
4. Analyze a memory cell and apply for organizing larger memories

COURSE OUTCOMES

1. Understand the different switching algebra theorems and apply them for logic functions.
2. Define the Karnaugh map for a few variables and perform an algorithmic reduction of logic functions.
3. Define the following combinational circuits: buses, encoders/decoders, (de)multiplexers, exclusive-ORs, comparators, arithmetic-logic units.
4. Understand the bistable element and the different latches and flip-flops.
5. Understand sequential circuits, like counters and shift registers.

UNIT-I	**NUMBER THEORY AND LOGIC SIMPLIFICATION**	**Classes: 09**

Number systems like binary, octal, hexadecimal and r's and r-1's complements, Review of Boolean Algebra and De Morgan's Theorem, SOP & POS forms, Canonical forms, Karnaugh maps up to 6 variables, Binary codes, Code Conversion.

UNIT-II	**COMBINATIONAL LOGIC DESIGN**	**Classes: 09**

MSI devices like Comparators, Multiplexers, Encoder, Decoder, seven-segment Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, and ALU.

UNIT-III	**SEQUENTIAL LOGIC DESIGN**	**Classes: 09**

Ripple and Synchronous counters, Shift registers, Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation.

UNIT-IV	**LOGIC FAMILIES AND SEMICONDUCTOR MEMORIES**	**Classes: 09**

TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, ECL, CMOS families and their interfacing, Memory elements like SRAM and DRAM, Concept of Programmable logic devices like PAL and PLA.

UNIT-V	**VLSI DESIGN FLOW**	**Classes: 09**

Introduction to HDL, Data types and objects, different modeling styles in VHDL, Dataflow, Behavioral and Structural Modeling, Synthesis and Simulation VHDL constructs and programs for combinational and sequential circuits including test-bench programming.

TEXT BOOKS:

1. R.P. Jain, "Modern digital Electronics", Tata McGraw Hill, 4th edition, 2009.

2. Douglas Perry, "VHDL", Tata McGraw Hill, 4th edition, 2002.

REFERENCE BOOKS:

1. W.H. Gothmann, "Digital Electronics- An introduction to theory and practice", PHI, 2nd edition ,2006.

2. D.V. Hall, "Digital Circuits and Systems", Tata McGraw Hill, 1989

3. Charles Roth, "Digital System Design using VHDL", Tata McGraw Hill 2nd edition 2012.

WEB REFERENCES:

1. www.wikipedia.org
2. www.pa.msu.edu
3. www.tutorvista.com
4. www.globalspec.com
5. www.ee.bilkent.edu.tr

E-TEXT BOOKS:

1. http://www.site.uottawa.ca/~petriu/Digital-Logic.pdf
2. http://uav.ece.nus.edu.sg/~bmchen/courses/EG1108_Digital.pdf
3. http://info.iet.unipi.it/~luigi/biomedica/sito/cosc205.pdf

MOOC Course

1. https://onlinecourses.nptel.ac.in/noc18_ee33/preview
2. https://onlinecourses.nptel.ac.in/noc18_ee34/preview